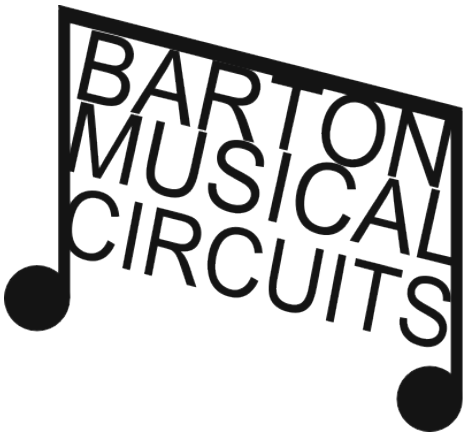


CV Arpeggiator Rev 1

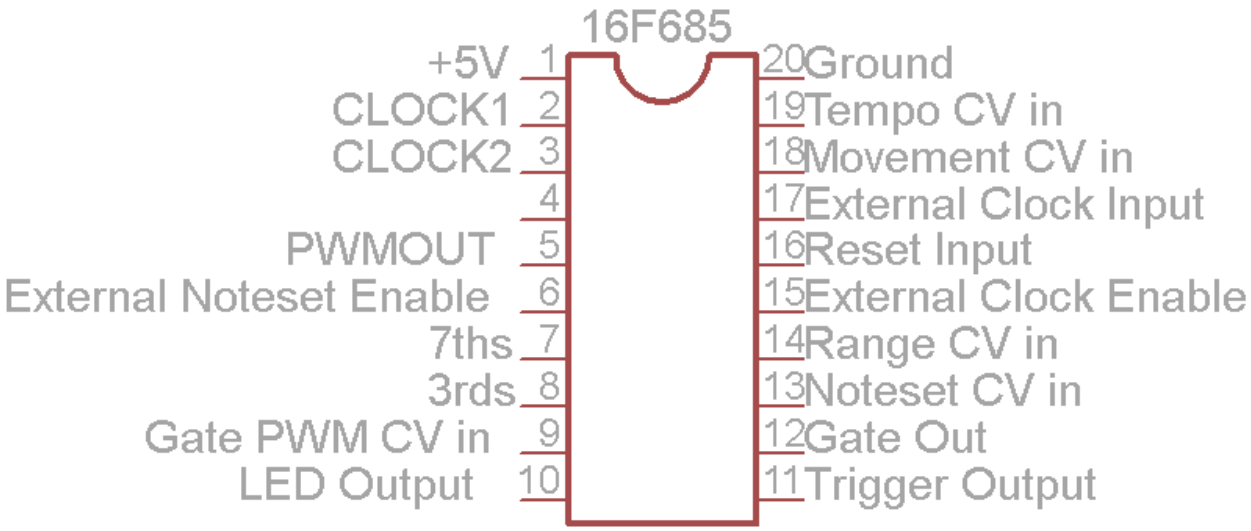
Last updated 6-11-2011

The CV Arpeggiator is a modular synth project used for creating arpeggios of control voltage. It utilizes a custom programmed PIC 16F685 micro controller. It includes an internal voltage controlled clock

I. The Chip

Section A - Pin-out.

Diagram 1:



Pins 9, 13, 14, 18 and 19 are used as CV inputs. DC voltages between 0 and +5V are used to control various parameters of the chip. These pins should be connected to a voltage source and decoupling caps connected to ground.

Pins 10, 11 and 12 are digital outputs, these toggle between 0 and +5V. These pins should be connected to build out resistors.

Pins 6, 7, 8, 15, 16 and 17 are digital inputs, which respond to pulses and toggles between 0 +5V. These pins should be connected to a voltage source and either pull-up or pull-down resistors.

Pin 5 is the pulse width modulator output, which in this circuit is used as a digital to analog converter. It is connected to a low pass filter.

Pins 2 and 3 are connected to a 20mhz crystal oscillator, which provides a time reference for the micro-controller.

Pins 1 and 20 connect the chip to the power supply. A decoupling cap should be placed between them.

Section B. Functional Descriptions

1. Note Generator Functions.

The note generator portion of the chip is controlled via 2 events and 3 parameters. These parameters and events control the output of the PWM which when filtered through a low-pass filter result in Arpeggiated control voltages

The two events which control the note generator are:
1.Clock Events
2.Reset Events

Clock *events control when the note generator changes notes. These come from the internal clock/divider.*

Reset *events control when the note generator goes back to the root note of the arpeggio. These can only be inputted from an external source. A +5V pulse on pin 16 causes a reset.*

The three parameters which control the note generator are:
1.Range
2.Movement
3.Note set

Range *limits the number of octaves the note generator can use. The following table displays what voltage ranges inputted to pin 14 will result in what octaves.*

Voltage Inputted	**Range**
0-1V	*1 octave range*
1.1V - 2V	*2 octave range*
2.1V-3V	*3 octave range*
3.1V-4V	*4 octave range*
4.1V-5V	*5 Octave range*

Movement *controls how the note generator moves through the note set; whether to generate the top or bottom note of a note set after a reset event and how to react when reaching the bottom or top. It is also has a "random" function which moves through a note set at random. The following table displays the various modes of movement available at what voltages on pin 18.*

Voltage	**Name**	**On Reset Goes to**	**At End of Note set**
0-.7V	*Up/Down*	*Bottom of note set*	*Reverses direction*
.8-1.4V	*Up Repeating*	*Bottom of note set*	*Goes back to bottom*
1.5-2.1V	*Down Repeating*	*Top of note set*	*Goes back to top of note set*
2.2-2.8V	*Pendulum*	*Bottom of note set*	*Holds note for 1 extra clock event at end, then reverses direction, on both bottom and top.*
2.9-3.5V	*Up and stay*	*Bottom of note set*	*Holds note until reset*
3.6-4.2V	*Down and stay*	*Top of note set*	*Holds note until reset.*
4.2-5V	*Random*	*Random note*	*n/a*

Note set refers to the musical notes contained in the arpeggio. Unlike the range and movement parameters, which are controlled exclusively by voltages, note set can be controlled either by an voltage exclusively or a voltage and a pair of digital inputs. A third digital input on pin 6 is used to change between methods of controlling note set

When pin 6 is held at 0V, a voltage is used exclusively to control note set, the following table shows what note sets are available at what voltages on pin 13.

Voltage	**Root**	**Minor 3rd**	**Major 3rd**	**5th**	**Minor 7th**	**Major 7th**
0-.6V	*Yes*	*No*	*Yes*	*Yes*	*No*	*No*
.6-1.2V	*Yes*	*Yes*	*No*	*Yes*	*No*	*No*
1.2-1.9V	*Yes*	*No*	*Yes*	*Yes*	*No*	*Yes*
2.0-2.5V	*Yes*	*Yes*	*No*	*Yes*	*Yes*	*No*
2.6-3.1V	*Yes*	*No*	*Yes*	*No*	*No*	*Yes*
3.1-3.8V	*Yes*	*Yes*	*No*	*No*	*Yes*	*No*
3.9V-4.4V	*Yes*	*No*	*No*	*Yes*	*No*	*No*
4.5V-5V	*Yes*	*No*	*No*	*No*	*No*	*N*

When pin 6 is held at +5V, pins 7 and 8 are used in conjunction with the voltage on pin 13. When pin 7 is held at +5V the 3rd in the note set is major, when held at 0V the 3rd in the note set is minor. Pin 8 controls the 7ths using the same logic. The following table shows what base note sets are used depending on what voltage is on pin 13.

Voltage	**Root**	**3rd**	**5th**	**7th**
0-.6V	*Yes*	*Yes*	*Yes*	*No*
.6-1.2V	*Yes*	*Yes*	*No*	*No*
1.2-1.9V	*Yes*	*Yes*	*Yes*	*Yes*
2.0-2.5V	*Yes*	*Yes*	*No*	*Yes*
2.6-3.1V	*Yes*	*No*	*Yes*	*Yes*
3.1-3.8V	*Yes*	*No*	*No*	*Yes*
3.9V-4.4V	*Yes*	*No*	*Yes*	*No*
4.5V-5V	*Yes*	*No*	*No*	*No*

So, when pin 7 is held at +5V, pin 8 is held at 0V and a voltage of 1.6 is present on pin 13, it will result in an note set of Root, Major 3rd, 5th and Minor 7th; also known as a dominant 7th chord.

2.Internal Clock/Divider Functions.

To generate clock events for the note generator an internal clock or divider is used. When Pin 15 is held at +5V the internal clock is used, when held at 0V the internal divider is used.

The internal clock has three hardware outputs and two parameters.

The three hardware outputs are
1.Trigger
2.Gate
3.Indicator LED

The two parameters are:
1.Tempo
2.Gate PWM

Trigger *outputs a+5V pulse on pin 11 lasting roughly 5ms whenever the clock generates a new note event.*

Gate *outputs a +5V pulse on pin 12 whenever the clock generates a new note event, the duration of the pulse is dependent on the gate PWM parameter or gate length parameter.*

Indicator LED *outputs a +5V pulse on pin 10 in unison with the Gate output.*

Tempo *controls the rate at which note events are generated. A voltage on pin 19 controls the tempo, it is continuously variable, thus no table is needed to explain.*

Gate PWM *controls the pulse width of the gate/LED. A voltage on pin 9 sets the PWM. The length of the gate is determined by the voltage on pin 9 and the period (amount of time between clock events) of the clock. If .5V were inputted on pin 9, and the tempo had been set to a period of 100ms, the resulting gate length would be 10ms. If 2.5V was present on pin 9 with the same tempo the gate length would be 50ms.*

The internal divider shares the same outputs as the internal clock, but the 2 parameters are replaced and an event is added.

The new parameters are:
1.Division.
2.Gate Length

The new event is the **external clock.** *When a +5V pulse is inputted to pin 17 this causes an external clock event.*

Division *determines how many external clock events it takes to cause a clock event. A voltage on pin 19 selects the division rate. The following table shows what voltages result in what division rates.*

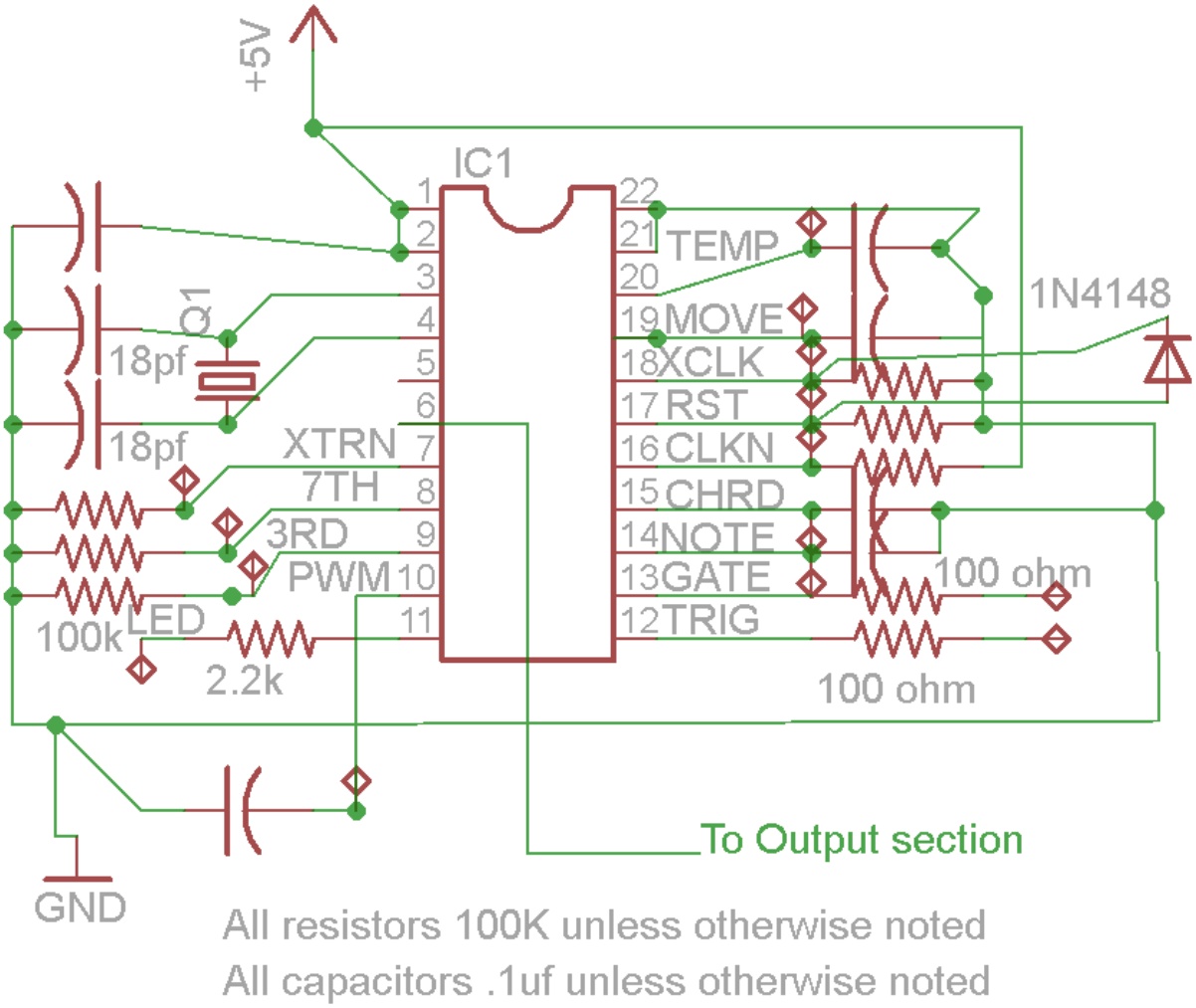
Voltage	**Divide by**
0-.6V	*1*
.6-1.2V	*2*
1.2-1.9V	*3*
2.0-2.5V	*4*
2.6-3.1V	*8*
3.1-3.8V	*16*
3.9V-4.4V	*32*
4.5V-5V	*64*

Gate Length *determines the actual amount of time a gate pulse lasts. It is not dependent on any other parameters, only the voltage on pin 9.*

II The PCB

A. Schematic/Summary of IC1 and Surrounding Circuitry

Diagram 2:



The first thing that should be noted is that while earlier we described the chip as having 20 pins, this diagram shows 22 pins. The board is laid out with 22 pins for IC1 so that builders who buy 8 pin and 14 pin IC sockets in large quantities can use what's on hand instead of buying the slightly less common 20 pin sockets. When inserting your chip into the socket, make sure to leave the spaces for pins 1 and 22 empty. For the following description of the circuit, I'll be referring to pin numbers as they appear on diagram 2.

IC1 is supplied power through pins 1 and 2 and a ground reference is established through pins 22 and 21. Q1 is a 20mhz crystal oscillator which provides an internal timing reference for the chip, it connects to pins 3 and 4, which are also connected to 18pf caps to ground which stabilize the oscillator.

All of the analog input pins (10, 14, 15, 19 and 20) have .1uf decoupling caps to ground which stabilize the control voltages. These pins are also connected to wiring pads for them to interface with their voltage sources.

The digital inputs on pins 7, 8, 9, 17 and 18 have 100k pull-down resistors connected to ground. These keep the pins at 0V until a positive pulse is inputted from the wiring pads. Digital input pin 16 uses a 100k pull-up resistor connected to +5V, this leaves the internal clock normally on, until the wiring pad is connected to ground.

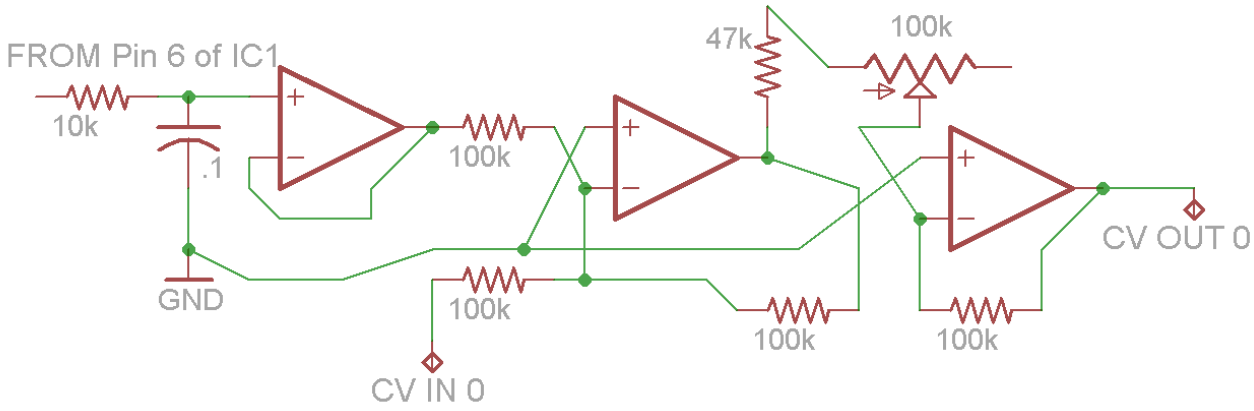
The 1N4148 diode ensures that whenever a reset pulse is sent a clock pulse is sent simultaneously.

The digital outputs on pins 12 and 13 have 100 ohm build-out resistors in addition to wiring

pads. The digital output on pin 11 uses a 2.2K current limiting resistor, though a different value can be used to adjust brightness of the LED. The wiring pad is intended to be connected to the anode (positive terminal) of an LED while the cathode is connected off board to ground.

B. Schematic/Summary of Output Circuitry

Diagram 3:



The PWM output from the micro-controller is filtered by the 10K resistor and the .1uf capacitor to ground, and then buffered by the first op-amp.

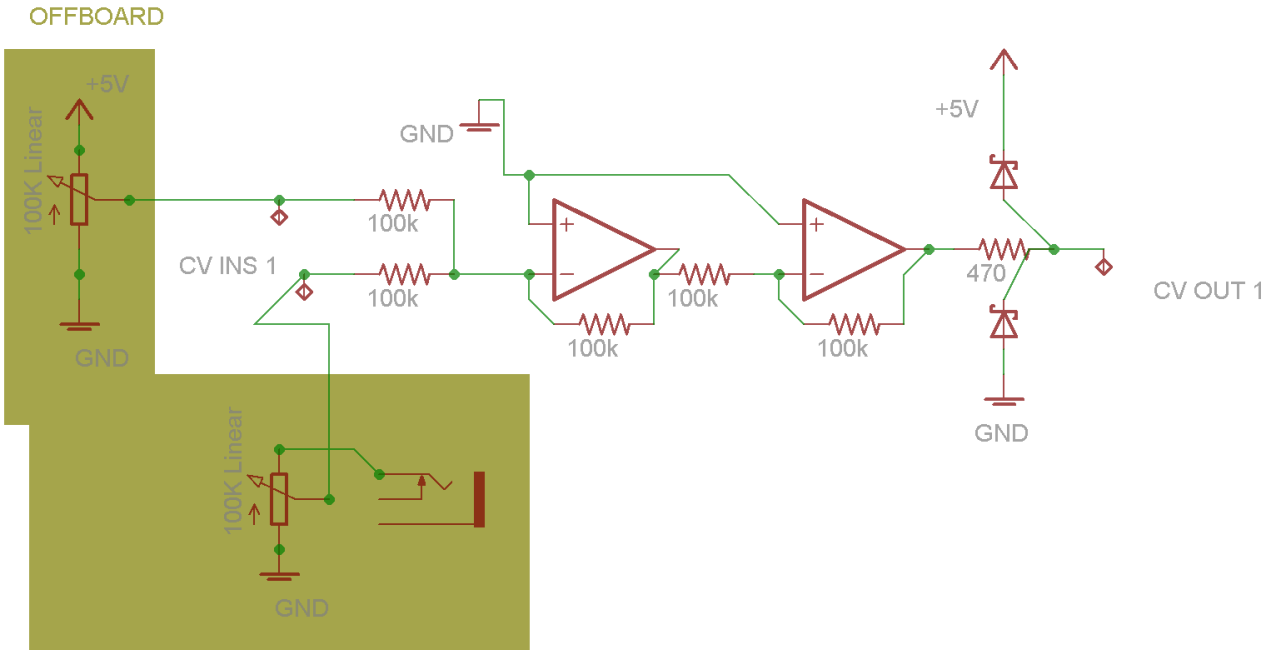
The next op amp acts as an inverting voltage summer. The voltage inputted at CV IN 0 is summed with the filtered output from IC1.

The final op-amp is an inverting gain stage. The trim pot should be adjusted so that the voltage outputted at wiring pad CV Out 0 is +5V when no voltage is inputted on CV IN 0 and the range pot is set to full rotation and movement is set to "up and stay" mode.

As a word of warning, because the final voltage is the sum of the output of IC1 and whatever is inputted at CV IN 0, output voltage can potentially be as high as +15V, so be careful with what you connect the circuit to.

C. Schematic/Summary of CV inputs.

Diagram 4:



This section is repeated twice on the PCB, once with pads marked "CV INS 1" / "CV OUT1"

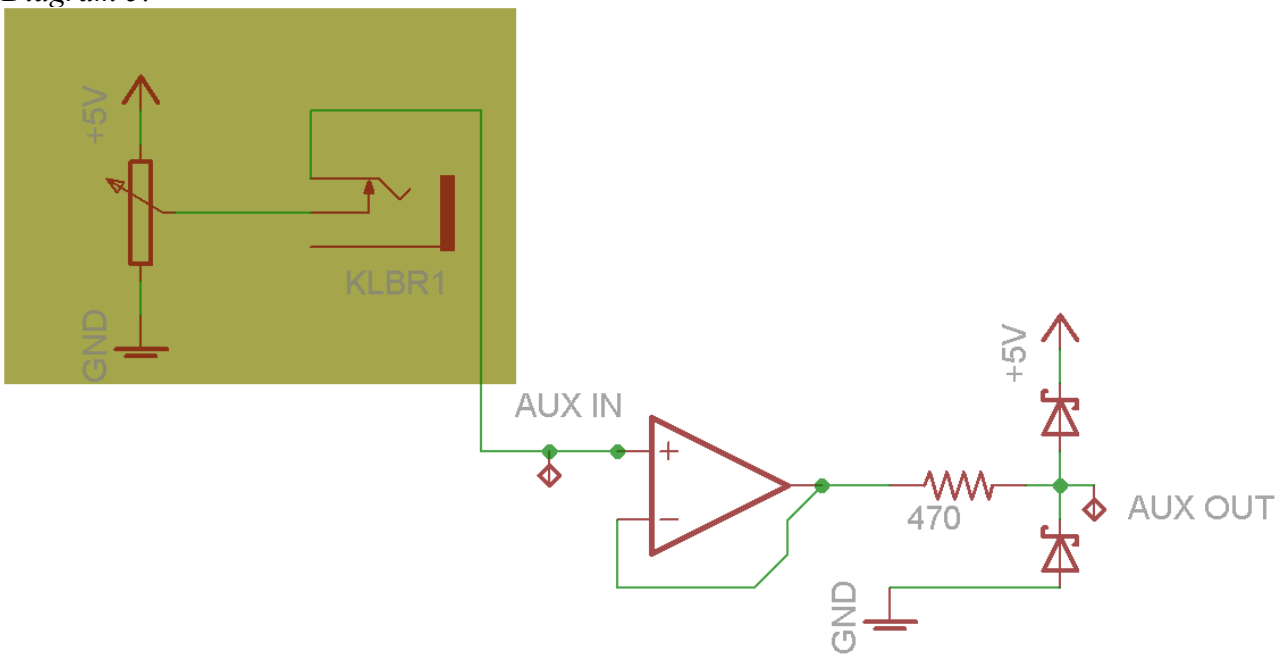
and once with pads marked "CV INS2" / "CV OUT2". The sections in yellow in the above diagram refer to off-panel wiring.

A voltage is being inputted through the jack on the bottom of the diagram, which is then being attenuated by a potentiometer set up as a voltage divider. This is being mixed with the output of another voltage divider on the left.

The two op amps act as a mixer, then inverting gain stage, just like in the output section. The second op-amp feeds 470 ohm build-out resistor which is then connected to 2 Schottky diodes. These diodes limit the voltage on CV OUT 1 to a range which won't damage IC1 or cause erratic behavior.

Use a jumper wire to connect CV OUT 1 to any of the CV inputs on IC1. This circuit allows one to use external control voltage sources to control parameters of the Arpeggiator.

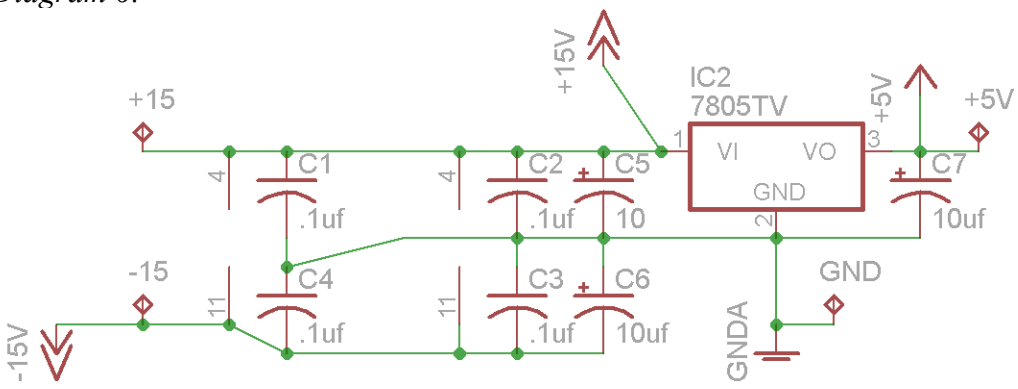
Diagram 5:



The above circuit is also used for limiting external control voltages, but does not have voltage mixing capabilities. A pot is connected to the switch of a switching jack so that when no external CV is plugged into the jack the pot is used to control the parameter, but when a jack is plugged in the external control voltage takes over.

D.Schematic/Summary of Power Supply

Diagram 6:

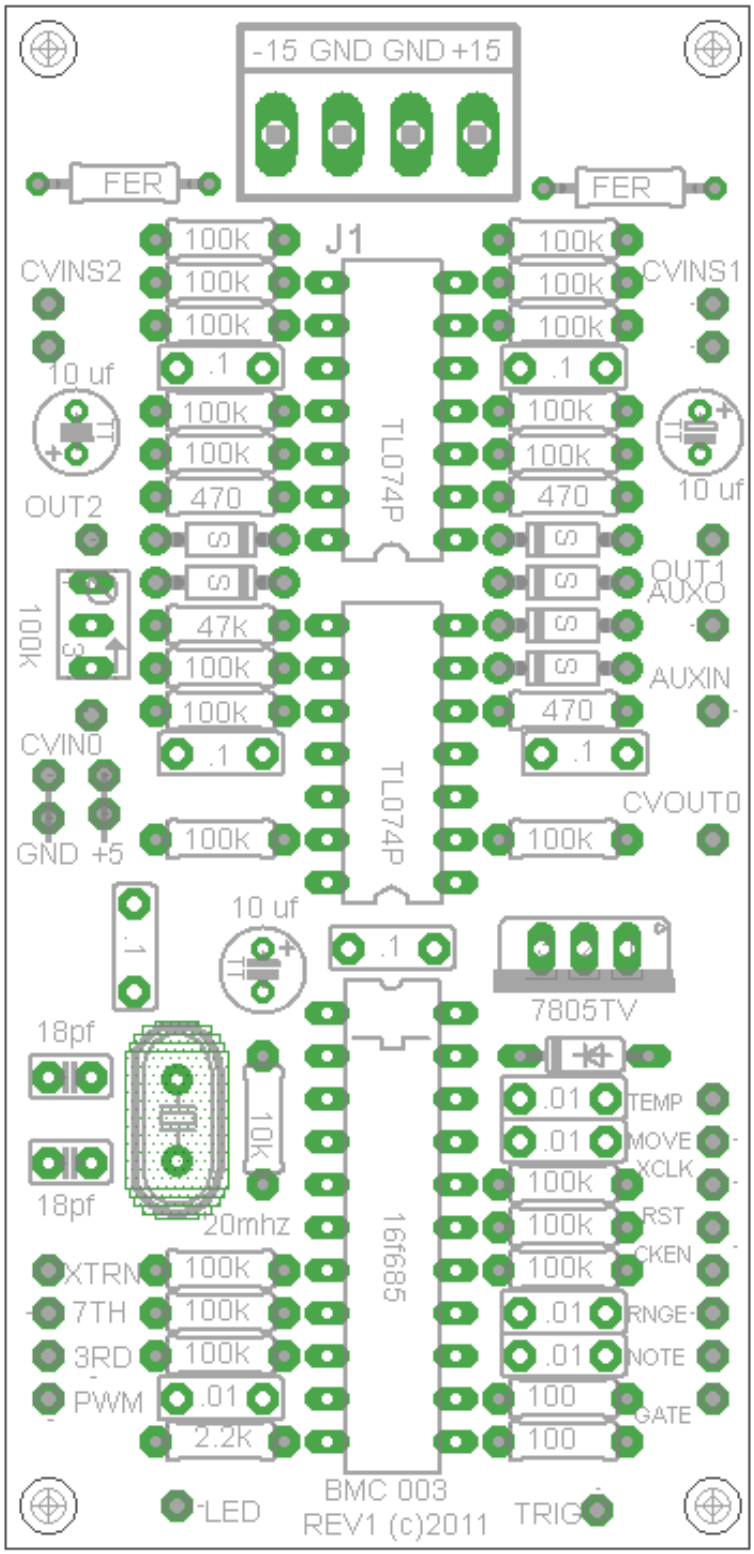


The power supply is connected to the supply rails of the modular case through the wire pads marked +15, -15 and GND. The +15V supply is then fed into a voltage regulator to produce the

+5V supply. The +/-15V rails and +5V rails are filtered by 10uf electrolytic filter caps. The two quad op-amp ICS also have decoupling .1uf capacitors near the supply pins on each IC. There are additional wire pads for +5V and GND supplies for connecting with off board components.

E. The Board/ Wiring Options

Diagram 7:



Note that on the board, the 16f685 is oriented in the opposite direction as the two TL074s and that the electrolytic capacitor in the top left corner is oriented in the opposite direction as the other two.

All Schottky type rectifiers are marked with an "S."

There are several options for wiring up your Arpeggiator module

1.Digital Note set Controls Always on/off.
If you plan on never using the digital note set controls replace the 100K pull down resistor next to the wire pad marked "XTRN" with a link. If you plan on always using the digital note set controls, wire a jumper from the wire pad marked "XTRN" to one of the pads marked "+5V"

2.Input For Voltage Parameter Controls.
Parameters controlled by a voltage can get their voltages from three sources:

A. A potentiometer wired as a voltage divider. *A set of pads connecting to the +5v supply and ground are on the left hand side of the board. Wire a connection between +5v and the pot's counter clockwise solder lug, and a connection between ground and the pot's clockwise solder lug. Wire the middle solder lug to the wire pad for the parameter you are controlling. Jumper the +5v supply and ground supply connections from pot to pot.*

B. A potentiometer wired as a voltage divider, mixed with external CV. *Diagram 4 shows a schematic of this. Wire one pot like as described in method A, connect the middle lug to one of the pads marked CVINS1. Wire the tip of a CV input jack to the counter clockwise lug of a second pot, wire ground to the clockwise lug of this pot and wire it's middle lug to the other CVINS1 pad. Wire a jumper from wire pad "OUT1" to the wire pad for the parameter you are trying to control. This is especially useful for the tempo and gate pwm parameters.*

C.Normally a potentiometer wired as a voltage divider, with external CV optional. *Diagram 5 shows a schematic of this. Wire a pot like in method A, but wire the middle pad to the lug for the tip's switch of a switching jack. Wire the tip of this jack to the wire pad marked "AUX IN" and wire a jumper from "AUXO" to the parameter you are trying to control.*

3.Automatically Disable Internal Clock.
The board is set up so that it is easy to set the module so that the Internal Clock is automatically disabled whenever an external clock signal is inputted for users using 2 conductor plugs. For your external clock input jack, use a stereo jack. Wire the pad marked "CKEN" to the ring (middle) connecter of the stereo jack. Wire the sleeve connecter of the stereo jack to ground, and wire the tip connecter to the wire pad marked "XCLK." This way whenever a plug is inserted, the sleeve of the plug will short the ring connecter to ground, disabling the clock.

F. Bill of Materials.

ICs

PART Value	*Quantity*
16f685	*1*
TL074 or similar in DIP 14 package	*2*
7805 in TO-220 package	*1*

RESISTORS. All 1/4 W.

PART VALUE	*Quantity*
100K	*20*

10K	*1*
100 ohm	*2*
2.2K	*1*
47K	*1*
470 ohm	*3*
100k trimpot	*1*
panel mount 100K linear potentiometer	*5-7 (depending on wiring options)*

CAPACITORS

PART VALUE	*Quantity*
.1uf. 5mm lead spacing. 16v or higher (REV1 boards accidentally refer to some of these as .01uf) Film or ceramic composition	*11*
18pf. 2.5mm lead spacing. 6v or higher	*2*
10uf electrolytic. 2.5mm lead spacing. 16v or higher	*3*

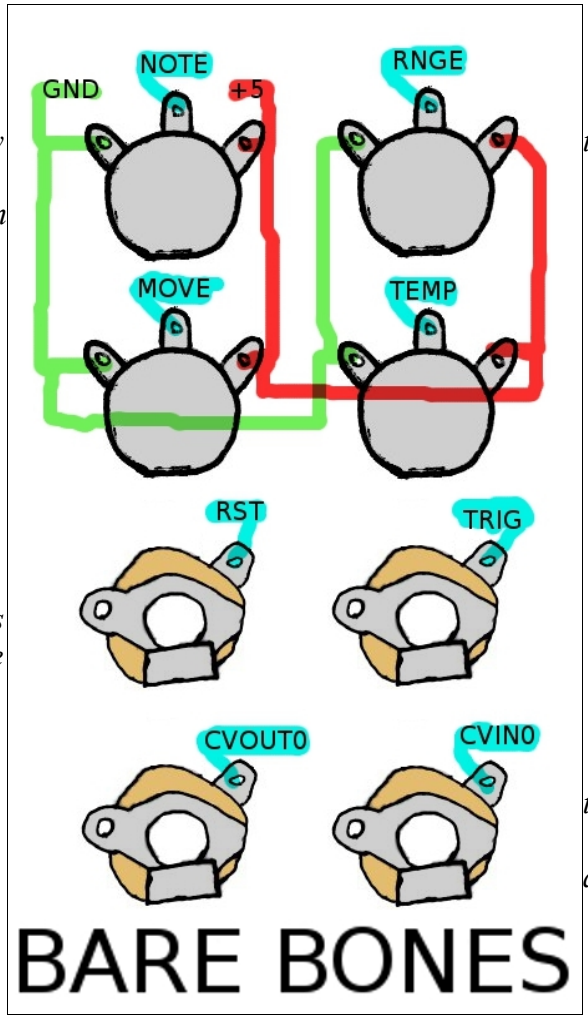
OTHER PARTS

PART	*Quantity*
Schottky Diode (SD101C was used in prototypes, but it's not critical)	*6*
1N4148 Diode	*1*
20mhz crystal oscillator 5mm lead spacing	*1*
LED	*1*
Mono Jack	*7*
Mono Switching Jack	*1 (optional, see wiring options)*
Stereo Jack	*1 (optional, see wiring options)*
Ferrite Bead (can be replaced with low 22 ohm resistor)	*2*

If you have any questions, please e-mail me at Michael@Bartonmusicalcircuits.com

G. Panel Wiring Examples

These examples are given to help give builders a clearer sense of how to build the arppegiator. There are many options, do not restrict yourself to one of these examples when deciding how build your module. The lines of a solid color indicate which terminals should be wired together on the panel.

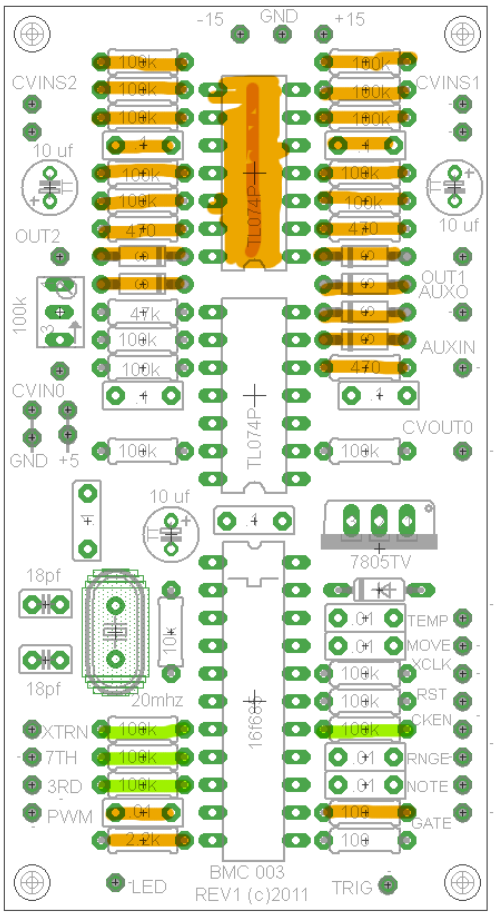


In all of these examples, text indicates which pad on the PCB that the terminal should be wired to. These diagrams are not drawn to scale.

Example 1. BARE BONES.

This layout uses no external voltage control, no external clock input and sacrifices the"gate" output and the PWM control along with it. This is as stripped down as you can get while still retaining the main functionality of the unit.

In addition to saving on panel space, a number of compononents on the board do not need be installed. In the diagram below, this are colored orange. Components in green can be replaced with jumper.



EXAMPLE 2. MICHAEL'S PROTOTYPE.

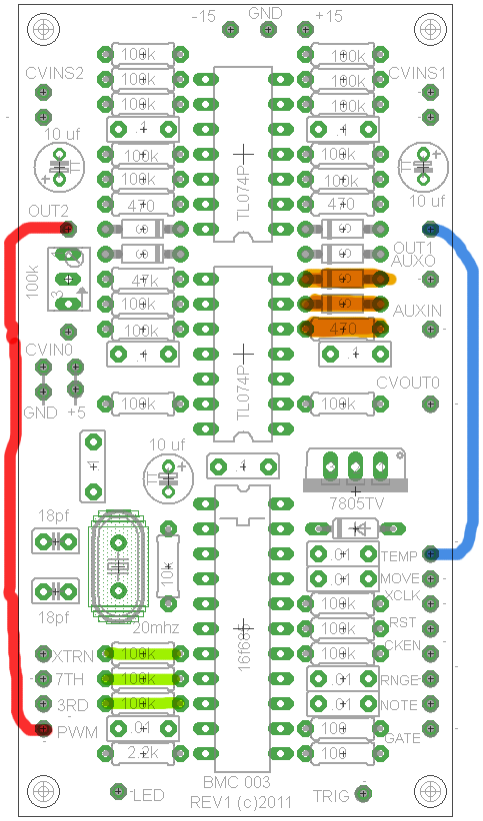
This layout is almost exactly like the one I originally used when building the prototype of the arppegiator (I later modified so I could test more functions of the module as I added them). In addition to the features of the "Bare Bones" layout, it adds the gate output and Gate PWM, an input for the external clock, an indicator LED and external CV inputs with attenuaters for the PWM and Tempo.

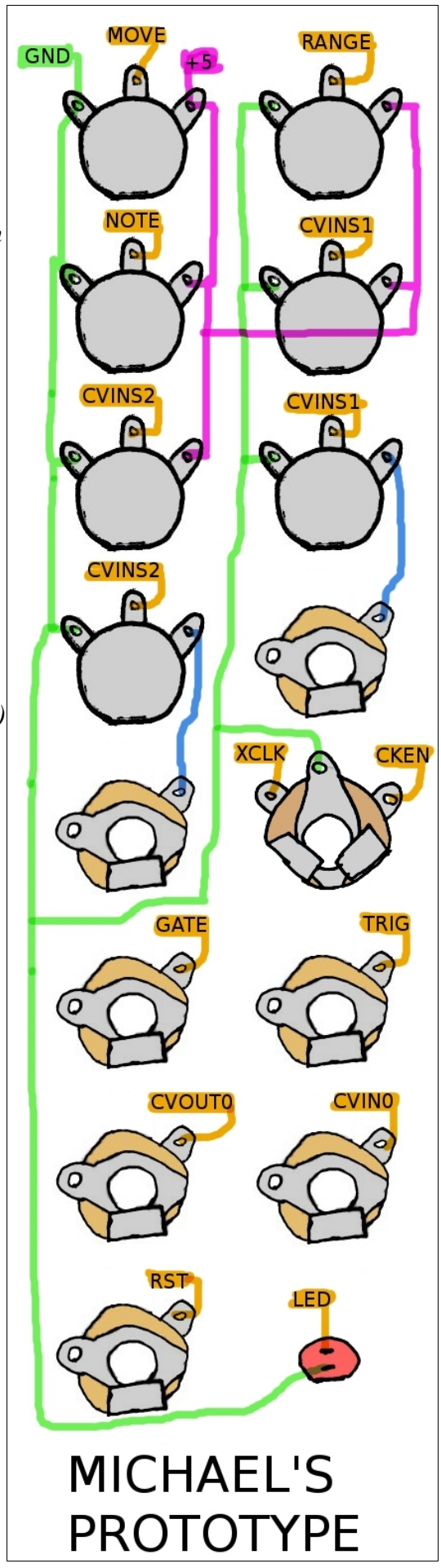
Note that, while two wires on this layout are marked as "CVINS1" these should not be tied together. On the board are two seperate wiring pads marked "CVINS1", one for each of these wires. The same goes for the two wires marked "CVINS2."

This layout automatically disables the internal clock when inserting an external clock, as was described in section E3 of this document.

If it's unclear from the diagram, the wire from the board to the LED should be attached to the anode (positive) terminal of the LED, and the cathode (negative) terminal should be wired to ground.

A jumper from "OUT2" to "PWM", and a jumper from "OUT1" to "TEMP" on the board are necessary for this layout. The components in orange can be left off of the board when using this layout, and the components in green can be replaced with jumpers





EXAMPLE 3. THE WORKS.

In addition to the features present in the last example, this layout adds external CV for Noteset, and external control for major/minor 3rds and 7ths.

The same notes regarding CVINS1 and CVINS2 from the last example apply to this example as well.

In addition to the onboard jumpers from the last example, another jumper wire from AUX0 to NOTE must be placed onboard.